AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

What is claimed is:

1. (Currently Amended) A device [[(10)]] for generating a noise signal, comprising:

a noise source [[(11)]] for generating intrinsic noise, ~~characterized in that~~ the noise source ~~(11) is~~ further comprising:

a noisy amplifier cell ~~(100)~~ having amplifying means ~~(103a, 103b),~~;

a load ~~(101a, 101b, 102a, 102b) connected to said~~ coupled to the amplifying means and a power supply[[,]]; and

a tail-current source ~~(104a, 104b) connected~~ coupled to grounding means and to the amplifying means ~~(103a, 103b)~~.

2. (Currently Amended) The device according to claim 1, wherein the amplifying means comprises a common-source amplifier ~~(103a, 103b)~~.

3. (Currently Amended) The device according to claim 2, wherein the common source amplifier ~~(103a, 103b)~~ comprises transistors ~~(103a, 103b)~~ having a differential topology.

4. (Currently Amended) The device according to ~~any of the claims 1-3~~, claim 1 wherein the load comprises cascoded transistors ~~(101a, 101b, 102a, 102b)~~.

5. (Currently Amended) The device according to ~~any of the claims 1-4~~, claim 1 wherein the load comprises resistors.

6. (Currently Amended) The device according to ~~any of the claims 2-5~~, claim 2 wherein the tail-current source ~~(104a, 104b)~~ is ~~connected~~ coupled to the amplifying means ~~(103a, 103b)~~ and the grounding means to provide common-mode feedback.

7. (Currently Amended) The device according to ~~any of the claims 1-6~~, claim 1 further comprising:

a first amplifier cell ~~(200)~~ being DC coupled to the noisy amplifier cell ~~(100),~~; and

the output terminals ~~(105a, 105b)~~ of the noisy amplifier cell ~~(100) are connected~~ coupled to respective input terminals ~~(206a, 206b)~~ of the first amplifier ~~(200)~~.

8. (Currently Amended) The device according to claim 7, wherein the design of the first amplifier ~~(200)~~ corresponds to the design of the noisy amplifier cell ~~(100)~~.

9. (Currently Amended) The device according to claim 7 ~~or 8~~, further comprising:

a differential amplifier ~~(300)~~ having first and second input terminals ~~(306a, 306b) connected~~ coupled to output terminals ~~(205a, 205b)~~ of the first amplifier ~~(200), said~~ the differential amplifier comprising amplifying means ~~(303a, 303b),~~;

a load ~~(301a, 301b, 302a, 302b) connected to said~~ coupled to the amplifying means and a power supply[[,]]; and

a tail-current source ~~(304a, 304b) connected~~ coupled to grounding means and to [[said]] the amplifying means.

10. (Currently Amended) The device according to ~~any of the claims 1-9~~, claim 1 wherein the load ~~(101a, 101b, 102a, 102b; 201a, 201b, 202a, 202b; 301a, 301b, 302a, 302b)~~, the amplifying means ~~(103a, 103b; 203a, 203b; 303a, 302b)~~, and the tail-current source ~~(104a, 104b; 204a, 204b; 304a, 304b)~~ of the noisy amplifier cell ~~(100)~~, ~~the first amplifier (200) and a differential amplifier (300),~~ comprises MOS (Metal Oxide Semiconductor) transistors.

11. (Currently Amended) The device according to ~~any of the claims 1-9~~, claim 1 wherein the load, the amplifying means, and the tail current source of the noisy amplifier cell ~~(100), the first amplifier (200) and a differential amplifier (300),~~ comprises BJT (Bipolar Junction Transistors) transistors.

12. (Currently Amended) The device according to ~~any of the claims 1-9~~, claim 1 wherein the load comprises PMOS transistors ~~(101a, 101b, 102a, 102b; 201a, 201b, 202a, 202b; 301a, 301b, 302a, 302b)~~, and the amplifying means and the tail-current source comprise NMOS transistors ~~(103a, 103b, 104a, 104b; 203a, 203b, 204a, 204b; 303a, 303b, 304a, 304b)~~.

13. (Currently Amended) The device according to ~~any of the claims 1-9~~, claim 1 wherein the load comprises NMOS transistors, and the amplifying means and the tail-current source comprises PMOS transistors.

14. (Currently Amended) The device according to claim ~~12 or~~ 13, wherein the width-over-length ratio [[(Z)]] of the transistors ~~(103a, 103b)~~ of the amplifying means is at least 3 times the width-over-length ratio of the transistors ~~(104a, 104b)~~ of the tail-current source, and the width-over-length ratio of the second transistor pair ~~(102a, 102b)~~ of the load is at least 3 times the size of the width-over-length ratio of the first transistor pair ~~(101a, 101b)~~ of the load.

15. (Currently Amended) The device according to claim ~~12 or~~ 13, wherein the width [[(W)]] of the transistors ~~(103a, 103b)~~ of the amplifying means and the transistors of the second transistor pair ~~(102a, 102b)~~ of the load is in the range of 2.5-125 μm, and the length [[(L)]] of [[said]] the transistors is in the range of 0.25-12.5 μm; the width and the length of the transistors ~~(104a, 104b)~~ of the tail-current source and the transistors of the first transistor pair ~~(101a, 101b)~~ of the load are in the range of 0.25-12.5 μm.

16. (Currently Amended) The device according to ~~any of the claims 1-15~~, claim 1 wherein input terminals ~~(106a, 106b)~~ of the amplifying means ~~(103a, 103b)~~ of the noisy amplifier cell ~~(100)~~ are short-circuited AC-wise to the grounding means.

17. (Currently Amended) The device according to ~~any of the claims 1-15~~, claim 1 wherein input terminals ~~(106a, 106b)~~ of the amplifying means ~~(103a, 103b)~~ of the amplifier cell ~~(100)~~ are short-circuited DC-wise to a fixed potential.

18. (Currently Amended) The device according to claim 7, further comprising:

the first amplifier cell being DC coupled to the noisy amplifier cell;

the output terminals of the noisy amplifier cell coupled to respective input terminals of the first amplifier; and

a DC compensation loop having a feedback filter ~~(15) connected~~ coupled to the output terminals ~~(205a, 205b)~~ of the first amplifier ~~(200)~~ and to the input terminals ~~(106b, 106a)~~ of the noisy amplifier ~~(100)~~, respectively.

19. (Currently Amended) The device according to claim 18, wherein the feedback filter [[(15)]] comprises first and second filters ~~(700a, 700b)~~ each comprising a high-frequency phantom zero capacitor ~~(C_z, 705)~~ providing phase compensation.

20. (Currently Amended) The device according to claim 18 ~~or 19~~, wherein the feedback filter [[(15)]] comprises two filters ~~(700a, 700b)~~ each comprising a first capacitor ~~(C_p, 707a-707e) connected~~ coupled to grounding means and a first resistor ~~(R1, 703) being connected~~ coupled to the output terminal of the filter ~~(700a, 700b)~~, a second resistor ~~(R_2, 702a-702b)~~ in parallel to the high-frequency phantom zero capacitor ~~(C_z, 705) connected~~ coupled to the output terminal of the filter ~~(700a, 700b)~~ and to a third resistor ~~(R_3, 701a-701b)~~ being ~~connected~~ coupled to the input terminal of the filter ~~(700a, 700b)~~.

21. (Currently Amended) The device according to claim 20, wherein the first capacitor ~~(C_p, 707a-707e)~~, the first resistor ~~(R1, 703)~~, the second resistor ~~(R_2, 702a-~~

~~702b)~~, the high- frequency phantom zero capacitor ~~(C_z, 705)~~, and the third resistor ~~(R_3, 701a-701b)~~ comprises MOS transistors.

22. (Currently Amended) The device according to claim 20, wherein the first capacitor ~~(C_p, 707a-707e)~~ comprises NMOS transistors, and the first resistor ~~(R_1, 703)~~, the second resistor ~~(R_2, 702a-702b)~~, and the third resistor ~~(R_3, 701a-701b)~~ comprises PMOS transistors.

23. (Currently Amended) The device according to claim 20, wherein the first capacitor ~~(C_p, 707a-707e)~~ comprises PMOS transistors, and the first resistor ~~(R_1, 703)~~, the second resistor ~~(R_2, 702a-702b)~~, and the third resistor ~~(R_3, 701a-701b)~~ comprises NMOS transistors.

24. (Currently Amended) The device according to ~~any of the previous claims, wherein~~ claim 1 further comprising:

[[an]] a noise source output terminal ~~(305) of said device (10);~~

~~is connected to~~ a random generating sequence device for generating a random sequence of bits coupled to the noise source output terminal; ~~device for generating a random sequence of bits (10),~~

the random generating sequence device further comprising:

[[an]] oscillating means having an input terminal ~~(409)~~ for receiving a bias as input, ~~connected to said~~ the oscillating means coupled to the noise source output terminal ~~(305)~~, the oscillating means ~~(13) comprises~~ further comprising at least one oscillator amplifier ~~(400a, 400b, 400c);~~

[[and]] amplifying means comprising at least one a differential amplifier ~~(500) connected to said~~ coupled to a corresponding the at least one oscillator amplifier~~, each oscillator amplifier (400a, 400b, 400c) and the differential amplifier (500) comprise~~;

[[an]] a load coupled to the amplifying means ~~(303a, 303b; 403a, 403b) protected~~ and to a power supply, the load being adapted to protect the amplifying means from interfering signals ~~by means of a load (301a, 301b, 302a, 302b; 401a, 401b, 402a, 402b) connected to said amplifying means and supply,~~; and

a tail current source ~~(304a, 304b; 404a, 404b) connected~~ coupled to [[said]] the amplifying means and grounding means.

25. (Currently Amended) The device of claim 1, further comprising an electronic apparatus ~~(1) comprising a device (10)~~ for generating a noise signal. ~~according to any of the claims 1-24.~~

26. (Currently Amended) The ~~electronic apparatus~~ device according to claim 25, wherein the electronic apparatus is one from the group consisting of a mobile radio terminal, a pager, a communicator, an electronic organizer [[or]] and a smartphone.

27. (Currently Amended) The electronic apparatus according to claim 25, wherein the apparatus is a mobile telephone [[(1)]].

28. (Currently Amended) [[An]] The device according to claim 1, the device being fabricated on an integrated circuit ~~comprising a device (10) for generating a noise signal according to any of the claims 1-24~~.

29. (New) The device according to claim 12, wherein the width-over-length ratio of the transistors of the amplifying means is at least 3 times the width-over-length ratio of the transistors of the tail-current source, and the width-over-length ratio of the second transistor pair of the load is at least 3 times the size of the width-over-length ratio of the first transistor pair of the load.

30. (New) The device according to claim 12 wherein the width of the transistors of the amplifying means and the transistors of the second transistor pair of the load is in the range of 2.5-125 μm, and the length of [[said]] the transistors is in the range of 0.25-12.5 μm; the width and the length of the transistors of the tail-current source and the transistors of the first transistor pair of the load are in the range of 0.25-12.5 μm.